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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/338,473	06/22/99	KIM Y	8836-116-(IB

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EXAMINER	
PATEL,G	
ART UNIT	**PAPER NUMBER**
2183	4

DATE MAILED: 07/02/01

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary

Application No.	Applicant(s)
09/338,473	Kim et al.
Examiner	**Art Unit**
Gautam R. Patel	2183

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *three* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on *Aug 3, 1999*

2a) ☐ This action is **FINAL.** 2b) ☒ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) *1-25* is/are pending in the applica

4a) Of the above, claim(s) _____ is/are withdrawn from considera

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) *1-25* is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claims _____ are subject to restriction and/or election requirem

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved.

12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

13) ☒ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

a) ☒ All b) ☐ Some* c) ☐ None of:

1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

*See the attached detailed Office action for a list of the certified copies not received.

14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

15) ☒ Notice of References Cited (PTO-892)

16) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)

17) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s). _____

18) ☐ Interview Summary (PTO-413) Paper No(s). _____

19) ☐ Notice of Informal Patent Application (PTO-152)

20) ☐ Other:

DETAILED ACTION

1. Claims 1-25 are pending for the examination.

Priority

2. Receipt is acknowledged of papers submitted under 35 U.S.C. § 119(a)-(d), which papers have been placed of record in the file.

NOTES & REMARKS

3. The lengthy specification has not ben checked to the extent necessary to determine the presence of all possible minor errors. For example specification page 3, line 4, "pointer 210" should read "pointer 20".

Applicant's cooperation is requested in correcting any errors of which Applicant may become aware in the specification.

Specification

4. The disclosure is objected for following reasons.

The title of the invention is neither precise nor descriptive. A new title is required which should include, using twenty words or fewer, claimed features that differentiate the invention from the Prior Art.

Correction is required.

Claim Objections

5. Claim 7 is objected for following reasons.

It seems that claim 7 has a typographical error. Claim 7, line 2 reads "first band", may be it should read "first bank"

Corrections and/or explanations are required.

Claim Rejections - 35 U.S.C. § 112

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

6. Claims 2-25 are rejected under 35 U.S.C. 112 first paragraph, as containing subject matter which was not described in the specification in such way as to which it pertains, or with which it is most nearly connected, to make and/or use the invention. [7.31.02].

It is not clear at all form the specification how content of a single stack pointer can insert a one-word item and remove a two-word item form the stack.

Similarly It is not clear at all form the specification how content of a main stack pointer can insert a one-word item and remove a two-word item from the stack.

7. The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

8. Claims 2-25 are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

It is not clear in claim 2, if content of a single pointer is inserting one-word and removing two-words simultaneously or a single pointer is inserting one-word and afterwards removing two-words.

a. as to claim 5, lines 1-3 "said stack storage control circuit one of increases and decreases the content of said stack pointer by one when .." is confusing and unclear.

b. Similarly it is not clear in claim 6, if content of the main pointer is inserting one-word and removing two-words simultaneously or a single pointer is inserting one-word and afterwards removing two-words. And what is the relationship of the first and second pointer with each other or with main pointer. Also in claim 6, lines 21-23 "in response to the decoding signals such that at least one of a one-word item and two-word item is one of inserted into" is on confusing and unclear.

Claim Rejections - 35 U.S.C. § 102

9. The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claim 1 is rejected under 35 U.S.C. § 102(b) as being anticipated by Kai et al., US. patent 5,287,309 (hereafter Kai).

As to claim 1, Kai discloses the invention as claimed [see Figs. 1-5] including an instruction decoder, a stack storage and a stack pointer circuit, comprising:

an instruction decoder [inherently present in any stack processing system] for generating a plurality of decoding signals, each of the plurality of decoding signals denoting one of a plurality of stack operations [pop and push] [col. 4, lines 14-20];

a stack storage [fig. 2, unit 5] comprising a plurality of storage locations, each of the plurality of storage locations being classified into one of at least two banks [fig. 2, units 10 and 11] [col. 4, lines 27-39];

a stack pointer circuit [fig. 2, unit 6] for pointing to at least one of the stack banks of the stack storage in response to at least one decoding signal to thereby cause a stack operation [col. 4, line 58 to col. 5, line 5];

Claim Rejections - 35 U.S.C. § 103

10. The following is a quotation of 35 U.S.C. § 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
>
> Subject matter developed by another person, which qualifies as prior art only under subsection (f) or (g) of section 102 of this title, shall not preclude patentability under this section where the subject matter and the claimed invention were, at the time the invention was made, owned by the same person or subject to an obligation of assignment to the same person.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. § 103, the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 C.F.R. § 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of potential 35 U.S.C. § 102(f) or (g) prior art under 35 U.S.C. § 103.

11. Claims 2-5 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Kai as applied to claim 1, in view of Koppala (US. patent 6,67,488) (hereafter Koppala).

As to claim 2, Kai discloses:

an instruction decoder [inherently present] for decoding an instruction and generating a plurality of decoding signals [POP and PUSH] [col. 4, lines 14-20];

a stack storage [fig. 1] comprising a plurality of locations for storing stack items [col. 1, lines 32-44];

a stack pointer [fig. 2, unit 6] for pointing to at least one of the locations of said stack storage [col. 4, lines 58-63]; and

a stack storage control circuit [fig. 2, units 7, 8 and 9] responsive to the decoding signals [col. 4, lines 21-26];

Kai disclose all of the above elements. Kai also discloses that a single pointer {SPM] can perform two operations simultaneously [PUSH and POP], and one signal is for pushing [or inserting] a word on the stack. Kai does not disclose that this single pointer can also POP [remove] two-word item form the stack, but Kai suggest that variation of the simultaneous POP and PUSH can be implemented, and this can be done by determination of the even and odd addresses and simple mathematical transformation [col. 2, lines 18-28; Kai]. However Koppala clearly discloses that control signal can be used for inserting a one-word item into said stack storage and removing a two-word item from said stack storage [col. 24, lines 27-30]. One of ordinary skill in the art would have realized that it is possible to execute two POP operation [or removing two-word item form the stack] instead of one PUSH and one POP operation in the system of Kai by simply transforming the logic as suggested by Kai. Also Koppala clearly discloses that "The most common stack manipulation for stack based computing system is to pop the two words from a stack and to push a data word onto the top of the stack" [col. 24, lines 29-32]. It would have been obvious to one of ordinary skill in the art at the time invention to have provided the a circuit of Kai with capability to remove two-word item form the stack storage as taught and suggested by Koppala, because it would have provided to a mechanism to execute the either two PUSH or two POP operation on the stack, thus making the stack operation much faster.

12. As to claim 3, Kai discloses:

each location of said stack storage is configured for storing a one-word item [inherently one-word is stored in stack memory].

13. As to claim 4, Koppala discloses:

a two-word item is one of inserted into and removed from two adjacent locations of said stack storage at a given time [col. 24, lines 21-40].

14. As to claim 5, Koppala discloses:

said stack storage control circuit increases and decreases the content of said stack pointer by one when the decoding signals indicate a one-word stack operation; and wherein said stack storage control circuit increases and decreases the content of said stack pointer by two when the decoding signals indicate a two-word stack operation [col. 24, lines 21-61].

15. As to claim 6, Kai discloses:

a stack storage [fig. 2, unit 5] including a plurality of locations, wherein each of the locations of said stack storage is assigned to one of a first [fig. 2, unit 10] and a second bank [fig. 2, unit 11] [col. 4, lines 27-39];

a main stack pointer [fig. 2, unit 6, SPM] for pointing to a location of said stack storage [col. 4, lines 59-63];

a first bank stack pointer [fig. 2, unit SPL] for pointing to a location assigned to said first bank [fig. 2, unit 10] [col. 5, lines 17-62];

a second bank stack pointer [fig. 2, unit SPL bar] for pointing to a location assigned to said second bank [fig. 2, unit 11] [col. 5, lines 17-62];

an instruction decoder [inherently present] for decoding a stack-based instruction and generating a plurality of decoding signals [col. 4, lines 14-20]; and

a stack pointer control logic circuit [fig. 2, units 7, 8 and 9] for controlling said first and second bank stack pointers in response to the decoding signals [col. 4, lines 21-26];

Kai disclose all of the above elements. Kai also discloses that a single pointer [SPM] can perform two operations simultaneously [PUSH and POP], and one signal is for pushing [or inserting] a word on the stack. Kai does not disclose that this single pointer can also POP [remove] two-word item form the stack, but Kai suggest that variation of the simultaneous POP and PUSH can be implemented, and this can be done by determination of the even and odd addresses and simple mathematical

transformation [col. 2, lines 18-28; Kai]. However Koppala clearly discloses that control signal can be used for inserting a one-word item into said stack storage and removing a two-word item from said stack storage [col. 24, lines 27-30]. One of ordinary skill in the art would have realized that it is possible to execute two POP operation [or removing two-word item form the stack] instead of one PUSH and one POP operation in the system of Kai by simply transforming the logic as suggested by Kai. Also Koppala clearly discloses that "The most common stack manipulation for stack based computing system is to pop the two words from a stack and to push a data word onto the top of the stack" [col. 24, lines 29-32]. It would have been obvious to one of ordinary skill in the art at the time invention to have provided the a circuit of Kai with capability to remove two-word item form the stack storage as taught and suggested by Koppala, because it would have provided to a mechanism to execute the either two PUSH or two POP operation on the stack, thus making the stack operation much faster.

16. As to claim 7 Kai discloses:

said stack storage comprises 2 n+1 locations, n being a positive integer, and wherein the first bank and the second bank each include 2 n locations [col. 4, lines 46-57].

17. As to claim 8 Kai discloses:

one of the first and second banks includes locations with addresses having a least significant bit of logic `0' and the other of the first and second banks includes locations with addresses having a least significant bit of logic ` 1' [col. 4, lines 40-45].

Allowable Subject Matter

18. Claims 9-16 and 17-25 are objected as being dependent upon a rejected base claim, but may be allowable if rewritten in independent form including all of the

limitations of the base claim and any intervening claims. This is subject to overcoming the 112 first and second rejection of the independent claims that these claims are dependent upon.

Other prior art cited

19. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a. Lynch (US. patent 4,424,563) "Data processor including a multiple word processing method and device".
b. Pawloski (US. patent 5,255,382) "Program memory expander for 8051-based micro controlled system".
c. Koino (US. patent 5,491,826) "Microprocessor having register bank and using a general purpose register as a stack pointer".
d. Saini (US. patemt 5,142,635) "Method and circuitry for performing multiple stack operations in succession in a pipelined digital computer".

Contact information

20. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Gautam R. Patel whose telephone number is (703) 308-7940. The examiner can normally be reached on Monday through Thursday from 7:30 to 6.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mr. Eddie P. Chan, can be reached on (703) 305-9712. The fax phone number for this Group is (703) 306-5404.

Any inquiry of a general nature or relating to the status of this application should be directed to the group receptionist whose telephone number is (703) 305-3900.

GRP

Gautam R. Patel
Patent Examiner
Group Art Unit 2183

June 20, 2001

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